64Kb Serial I²C nvSRAM

FEATURES

- **Two-Wire Serial Interface**
- **BI-directional Data Transfer Protocol**
- **1MHz Clock Rate**
- **Low Power Consumption**
- **Write Protection Pin for Hardware Data Protection**
- **Internal 8192 x 8b Organized**
- **Block rollover**
- **WRITE at Bus Speed**
- **Self-Timed PowerStore Cycle (8ms)**
- **Hardware Write-Protect**
- **Unlimited READ and WRITE Cycles**
- **100k PowerStore Cycles**
- **20-Year Non-volatile Data Retention**
- **3.0V to 3.6V Power Supply**
- **Extended Temperature Range**
- **8-pin 150 mil SOIC Packages**
- **RoHS-Compliant**

DESCRIPTION

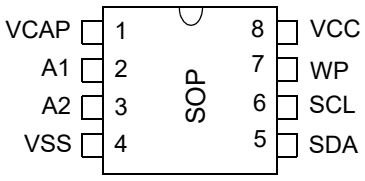
The Anvo-Systems Dresden ANV32A62ASE is a 64Kb serial SRAM with a non-volatile SONOS storage element included with each memory cell, organized as 8k words of 8 bits each. The devices are accessed by a two-wire bus. Up to 4 cascadable devices can share the common bus. The ANV32A62ASE is accessed via a two-wire interface consisting of Serial Data / Address (SDA) and Serial Clock (SCL). All STORE cycles are self-timed.

The serial nvSRAM provides the access and cycle times, easy to use and unlimited READ and WRITE endurance of a SRAM.

Data transfers automatically to the non-volatile storage cells when power loss is detected or in any brown out situation (PowerStore). As long as power will be supplied within operating conditions all data stay volatile in the SRAM cells.

WRITE Protection of data in upper quarter of address space of the memory occurs when the Write Protect pin is connected to V_{CC}.

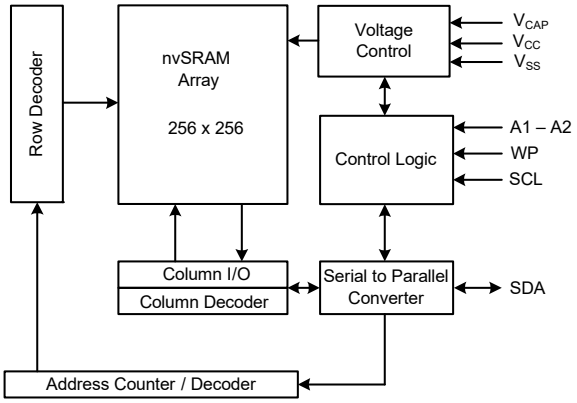
PIN CONFIGURATION



Top View

8-pin SOP 150 mil

BLOCK DIAGRAM



PIN DESCRIPTION

Signal Name	Signal Description
A1 - A2	Address Inputs
SCL	Serial Clock
SDA	Serial Data / Address
WP	Write Protect
VCC	Supply Voltage
VCAP	PowerStore Supply Voltage
VSS	Ground

Pin Description

Device Select Addresses (A2, A1): The 2 pins A1 - A2 are device address inputs to select 1 of up to 4 devices of the same type on the same SCL / SDA bus. To select one device the hard wired addresses on the 2 pins have to match with the related bits in the slave address.

Serial Data / Address (SDA): The SDA pin is a bidirectional pin for the data transfer. As output it is open drain and as input it will as Schmitt trigger to increase noise immunity. An external pull-up resistor is required to support the high level on the bus.

Serial Clock (SCL): The SCL input clocks in the data into the nvSRAM with the positive edge and with the negative edge the data clocked out of the device.

Write Protect (WP): The WP input pin controls the Write access to the upper 16Kb of the memory. When WP is connected to ground the whole nvSRAM can be written. If the pin is floating it will be internally pulled down to ground. When WP is connected to V_{CC} the upper 16Kb are read-only.

Memory Architecture

The ANV32A62ASE is a 64Kb serial nvSRAM 8Kb x 8 organized. It is using a standard two-wire interface (I²C) and is functional similar to serial EEPROMs or FRAM . The addressing requires a 13 bit address out of the 2-byte address of the two-wire protocol.

Two-wire Interface

The ANV32A62ASE is designed to support a bi-directional two-wire bus protocol. Figure 1 below shows a typical system configuration.
Any device sending data onto the bus is the transmitter and the target device is the receiver. The master controls the bus and is generating the clock for all devices on the bus. All controlled devices are slaves and the ANV32A62ASE is a slave.

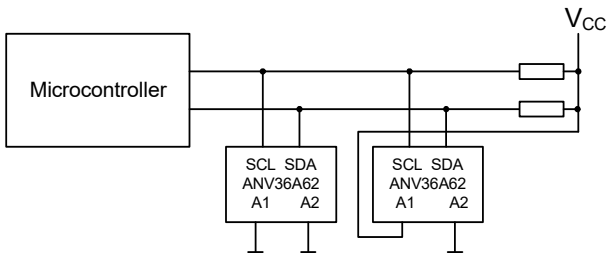


Fig.1: System configuration example

Stop Condition
Master must have the control over the two-wire bus, no memory READ can be in progress, to assert a stop condition. A stop condition is valid when the master drives SDA from low to high when SCL is stable high. All operations should end with such a stop condition. Any operation which is in progress will be aborted.

Start Condition:
A start condition is indicated when the master drives SDA from high to low while SCL is stable high. All commands should be preceded by a start condition.With a start condition any operation in progress can be aborted at any time.

Data Transfer:
All address and data transfers take place while SCL is high. Data on SDA may change only during SCL low phase. The SDA pin should not change while SCL is high. All data transfers occur with MSB first.

Acknowledge:
All addresses and data words are serially transmitted to and from the ANV32A62ASE in 8-bit words. During the 9th clock cycle the ANV32A62ASE sends a zero to acknowledge receipt of the byte or expect a zero from the master to send the next byte. If there is no acknowledge signal the condition is no-acknowledge and the operation is aborted.

Slave Address:
After start condition the first byte is the slave address. The slave address contains in the bits 7 to 4 the slave ID (1010), in the bits 3 to 1 the device select address bits and in bit 0 the selection for read or write operation. See Figure 2.

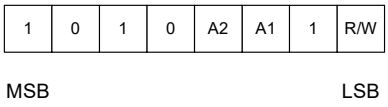


Fig. 2: Device Address

Addressing Overview:
The ANV32A62ASE uses the 2 device addresses A2 to A1 to allow up to 4 devices on the same bus. After acknowledge the device address from the selected device the master can send the 2 byte memory address to the bus for a write operation. Internally the 13 bit address will be latched. With each access the latched address will be incremented by 1. The current address is the value in the latch which is either a new written address or the address following the last access as long as power is supported or a new address is written in the latch.
Reads always use the current address. To start a random read a “dummy write” has to occur before.

Memory Reset:

The part can be reset by clocking up to 9 cycles and looking for SDA high in each cycle followed by start condition.

Device Operation

The ANV32A62ASE operates most similar like other two-wire interface memory products. Major differences are related to the nvSRAM technology, especially the PowerStore operation as explained below.

Power Up Recall:

During power up or after any low-power condition (V_{CC}<V_{RESET}), an internal RECALL request will be latched. When V_{CC} once again exceeds the sense voltage of V_{SWITCH}, a RECALL cycle will automatically be initiated and will take $t_{RESTORE}$ to complete.

During Power Up Recall operation, all input information will be ignored and SDA is high-Z.

Write:

A write operation requires a start condition first, the 8-bit device address with the LSB = 0 to select Write function, followed by the acknowledgment from the nvSRAM. Thereafter the first 8 address bits, where the first 3 bits are don't care, will be clocked in and after acknowledgement the second 8- address bits will be clocked in. After acknowledgment first 8-bit data word can be clocked in. An unlimited number of data bytes can be clocked in and will be stored volatile as long as the master doesn't send the stop condition. Before the nvSRAM sent a 0 to the bus for acknowledgement the internal address counter will be incremented by 1. When the end of the address range is reached internally, the address counter will wrap from 1FFFh to 0000h. The complete memory can be written with one write operation. With the stop condition a new READ or WRITE operation can be executed.
If the WRITE will not be terminated by a stop condition, all written data of the last byte will be ignored.
Every, with start and stop condition, completely executed write operation will store all volatile data to non-volatile with the next power down cycle. This is also valid for all written data of the current write operation and all prior written valid volatile data out of incomplete writes without stop condition.
When Write Protect pin is pulled to V_{CC} the upper 16Kb are write protected and the internal address counter will not increment addresses in this upper block.
Single byte writes and multiple byte writes, volatile and non-volatile, are illustrated in Fig. 3 to Fig. 6 below.

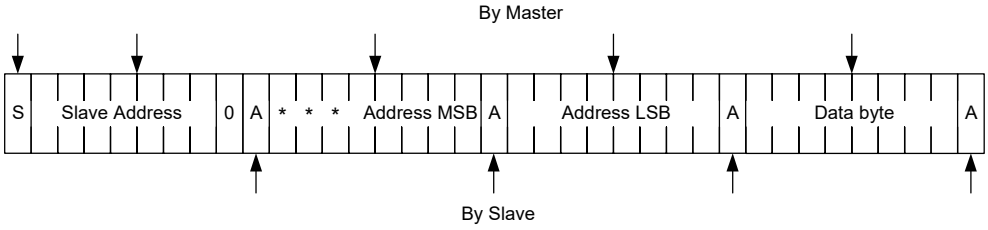


Fig.3: volatile single byte write

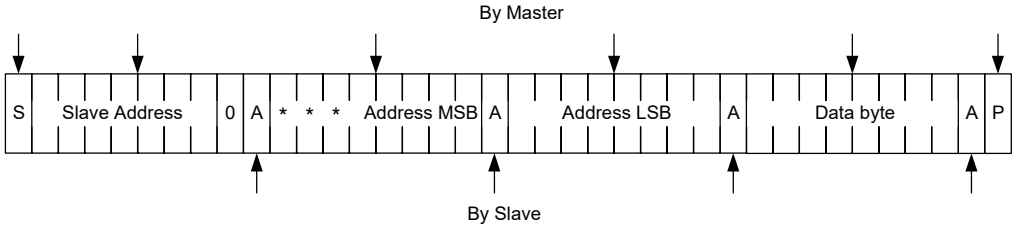


Fig. 4: single byte write

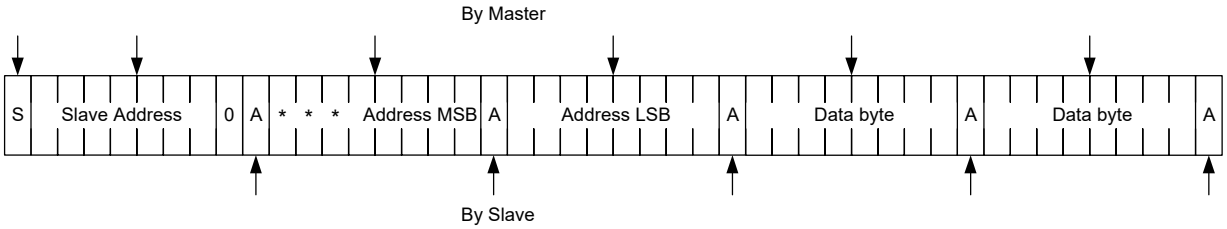


Fig. 5: volatile multiple byte write

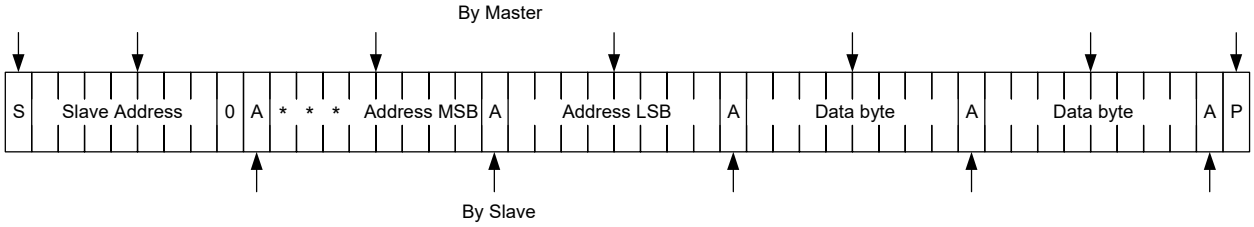


Fig. 6: non-volatile multiple byte write

Read Operation

There are 3 types of read operations:
- current address read
- sequential read
- random read

Current Address Read

The internal address counter maintains the last address of any completed write or read operation incremented by 1. This will be the address for the data byte which will be clocked out. The master has just to send the start condition followed by the slave address and LSB = 1. The Slave will acknowledge and clock out 8 data bits. To complete the current address read the master will not acknowledge in the 9th clock cycle and sent in the 10^{th} clock cycle a stop condition.
Fig.7 illustrates the current address read operation.

Sequential Read

Any Current Address Read is the first sequence of Sequential Read. After clocking out the first data byte the nvSRAM increments the internal address counter by 1 and after an acknowledgement from the master the next byte will be clocked out. Any acknowledgement from the master is a further start for clocking out the next sequential byte so that the complete memory can be read out independent what the start address was.
Fig. 8 illustrates the sequential read.

Random Read

Any random read requires a dummy byte write sequence to load the data word address. Once the device address and the data address are clocked in and acknowledged by the nvSRAM, the master has to generate a start condition again. Now the master can initiate a random read by sending the slave address with the read/write select bit =1. After acknowledgement by the slave it will clock out the first byte of data. If master doesn't acknowledge the data byte and send a stop condition the random read operation is finished. In case the master acknowledges the first data byte the slave will clock out the sequential next byte. This will continue as long as the master acknowledge each clocked out data byte.
Fig. 9 illustrates random read.

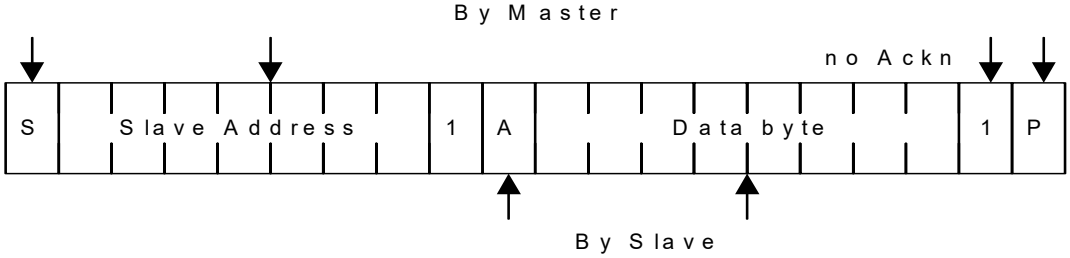


Fig. 7: Current Address Read

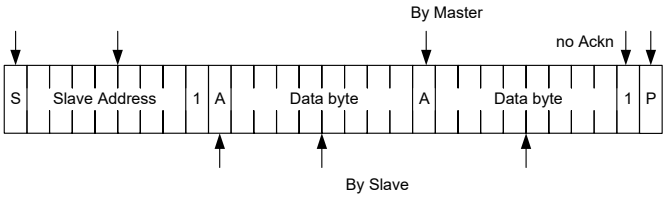


Fig. 8: Sequential Read

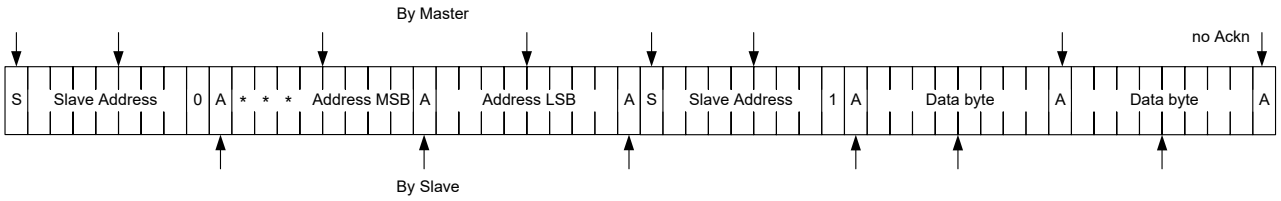


Fig. 9: Random Read

PowerStore Operation:

PowerStore operation is a unique feature of the SONOS technology that is enabled by default on the ANV32A62ASE.

During normal operation, the device will draw current from V_{CC} for circuit operation and to charge a capacitor connected to the V_{CAP} pin. This stored charge will be used by the chip to perform a single STORE operation in case of power down. If the voltage on the V_{CC} pin drops below V_{SWITCH}, the part will automatically disconnect the V_{CAP} pin from V_{CC}. A STORE operation will be initiated with power provided by the V_{CAP} capacitor.

If a WRITE operation is in progress all data of complete written pages are valid. Only the last incomplete written byte will be ignored. With the following Power Store execution these data become non-volatile.

Below, is shown the proper connection of the storage capacitor (V_{CAP}) for automatic store operation. Refer to the DC CHARACTERISTICS table for the size of V_{CAP}.

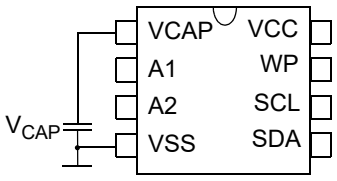


Fig. 10: PowerStore Cofiguration

To reduce needless non-volatile stores, Power Store operation will be ignored unless at least one WRITE operation has taken place since the most recent STORE cycle. The PowerStore Operation is valid for the complete memory array.

Power Up Recall:

During power up or after any low-power condition (V_{CC}<V_{SWITCH}), an internal RECALL request will be latched. When V_{CC} once again exceeds the sense voltage of V_{SWITCH}, a RECALL cycle will automatically be initiated and will take $t_{RESTORE}$ to complete.

During Power Up Recall operation, all commands will be ignored.

ABSOLUTE MAXIMUM RATINGS[a]

Voltage on Input Relative to Ground . . . . . .–0.5V to 4.5V
Voltage on Input Relative to VSS . . . . . .–0.6V to (VCC + 0.5V)
Temperature under Bias . . . . . –55°C to 125°C
Storage Temperature . . . . . –65°C to 150°C
Power Dissipation 0.5W
DC Output Current (1 output at a time, 1s duration) 15mA

a. Stresses greater than those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Operating Conditions

Symbol	Parameter	ANV32A62ASE		Unit
		Min.	Max.	
V_{CC}	Operating Voltage	3.0	3.6	V

DC CHARACTERISTICS

(V_{CC} / V = 3.0 - 3.6)

SYMBOL	PARAMETER	Extended		UNITS	NOTES
		MIN	MAX		
I_{CC1}[a]	Average V_{CC} Current at 1MHz		1	mA	$V_{IN} \le 0.2V_{CC}$ or $\ge 0.8V_{CC}$
I_{CC3}[a]	Average V_{CC} Current at 400 kHz		700	µA	$V_{IN} \le 0.2V_{CC}$ or $\ge 0.8V_{CC}$
I_{SB1}	V_{CC} Current Standby		200	µA	$V_{IN} \le 0.2V$ or $\ge (V_{CC} - 0.2V)$
I_{ILK}	Input Leakage Current		±3	µA	V_{CC} = max $V_{IN} = V_{SS}$ to V_{CC}
I_{OLK}	Off-State Output Leakage Current		±3	µA	V_{CC} = max $V_{IN} = V_{SS}$ to V_{CC},
V_{IH}	Input Logic “1” Voltage	$0.8V_{CC}$	V_{CC} + 0.5	V	All Inputs
V_{IL}	Input Logic “0” Voltage	V_{SS} – 0.5	$0.2V_{CC}$	V	All Inputs
R_{IN}	Address Input Resistance	50		KOHM	$V_{IN} = V_{IL}$
V_{OL}	Output Logic “0” Voltage		0.4	V	I_{OUT} = 2 mA
T_A	Operating Temperature	-40	105	°C	
C_{CAP}	Storage Capacitor	48	100	µF	6.3V
NV_C	PowerStore operations	100		K	
$DATA_R$	Data Retention	20		Years	@70 °C after last STORE operation

Note a: I_{CC1} and I_{CC3} are dependent on output loading and cycle rate. The specified values are obtained with outputs unloaded.

AC Characteristics

Switching Characteristics	Symbol	Min.	Max.	Unit
SCK Clock Frequency	f_{SCK}	0	1	MHz
Clock High Period[a]	t_{CH}	400		ns
Clock Low Period[a]	t_{CL}	600		ns
Input Rise Time[b]	t_R		300	ns
Input Fall Time[c]	t_F		100	ns
Clock Low to Data Out Valid	t_{AA}		550	ns
Bus Free before new Transition	t_{BUF}	500		ns
Start Condition Hold Time	$t_{HD\ STA}$	250		ns
Start Condition Set-Up Time	$t_{SU\ STA}$	250		ns
Data in Hold Time	$t_{HD\ DAT}$	0		ns
Data In Set-Up Time	$t_{SU\ DAT}$	100		ns
Stop Set-UP Time	$t_{SU\ STO}$	250		ns
Data Out Hold Time	t_{DH}	0		ns
nv-Write Cycle Time	t_{WR}		8	ms

a. $t_{CH} + t_{CL} \geq 1 / f_{SCK}$
b. $0.2V_{CC}$ to $0.8V_{CC}$
c. $0.8V_{CC}$ to $0.2V_{CC}$

AC TEST CONDITIONS

Input Pulse Levels	0V to 3V
Input Rise and Fall Times	≤ 10ns
Input and Output Timing Reference Levels	1.5V
Output Load	See Fig. 11

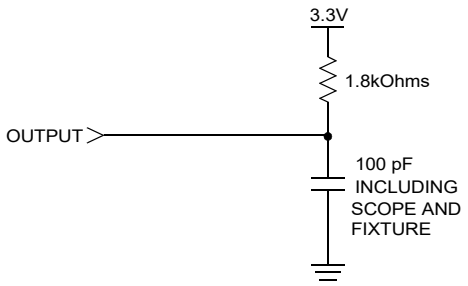


Fig. 11: AC Output Loading

CAPACITANCE (T_A = 25°C, f = 1.0MHz)

SYMBOL	PARAMETER	MAX	UNITS	CONDITIONS
C_{IN}	Input Capacitance	5	pF	ΔV = 0 to 3.3V
C_{OUT}	Output Capacitance	7	pF	ΔV = 0 to 3.3V

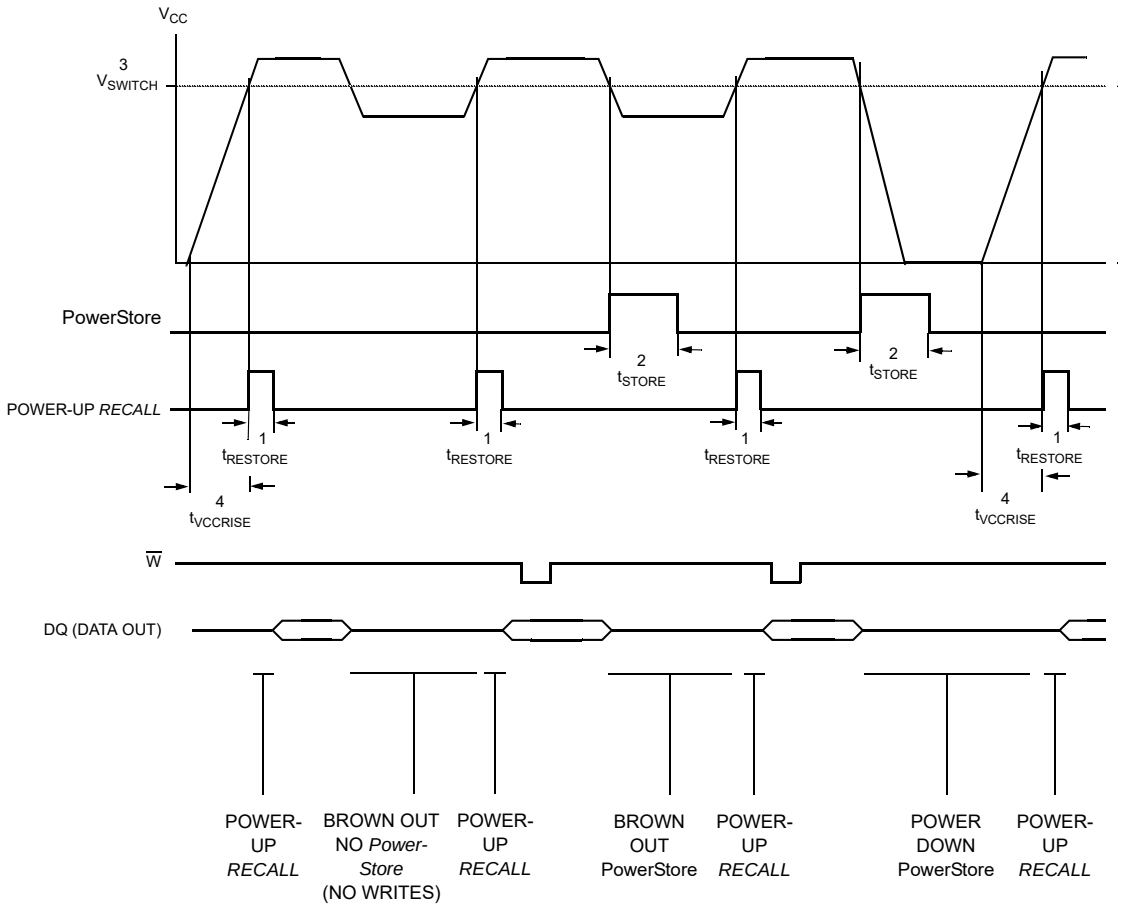
These parameters are guaranteed but not tested.

PowerStore/POWER-UP *RECALL*

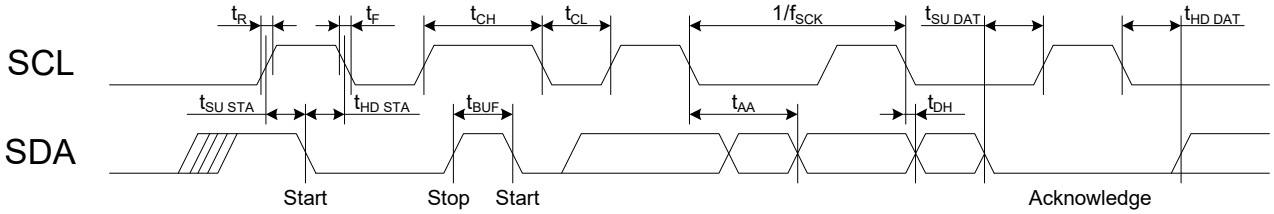
NO.	SYMBOLS		PARAMETER	ANV32A62ASE		UNITS
				MIN	MAX	
1	$t_{RESTORE}$[a]		Power-up *RECALL* Duration		200	µs
2	t_{STORE}		PowerStore Cycle time		8	ms
3	V_{SWITCH}		Low Voltage Trigger Level	2.7	2.95	V
4	$t_{VCCRISE}$		V_{CC} rise time	100		µs

a. $t_{RESTORE}$ starts from the time V_{CC} rises above V_{SWITCH}

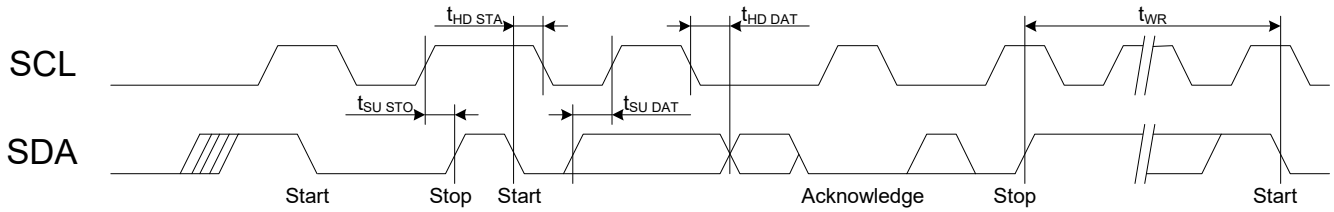
POWER-UP *RECALL and Brown Out*



Read Bus Timing



Write BusTiming



Product Versions

The ANV32A62ASE will be available with the feature sets:

- Supply voltage range 3.0 to 3.6V

Initial Delivery State

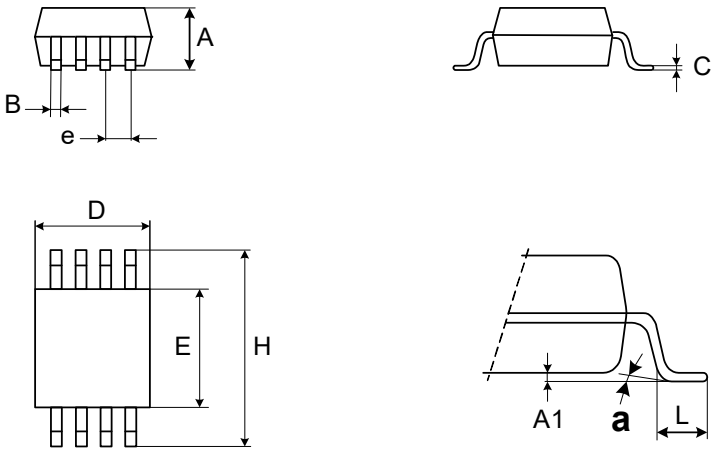
The device is delivered with non-volatile memory array „0“.

NOISE CONSIDERATIONS

The ANV32A62ASE is a high-speed memory and so must have a high-frequency bypass capacitor of approximately 0.1µF connected between V_{CC} and V_{SS}, using leads and traces that are as short as possible. As with all high-speed CMOS ICs, common careful routing of power, ground and signals will help prevent noise problems.

Package

8-pin 150mil SOIC



Symbol	mm			inches		
	typ..	min.	max	typ.	min.	max.
A		1.35	1.75		0.053	0.069
A1		0.1	0.25		0.004	0.010
B		0.33	0.51		0.013	0.020
C		0.19	0.25		0.007	0.010
D		4.80	5.00		0.189	0.197
E		3.80	4.00		0.150	0.157
e	1.27			0.050		
H		5.80	6.20		0.228	0.244
L		0.40	0.90		0.016	0.035
a		0°	8°		0°	8°

Ordering Information